List of Projects: 2025-26

-

SNo	Dept	Guide	USNs	Title	Status	Abstract
1	EC	Prof. Nisha G.R	4VP22EC008 4VP22EC009 4VP23EC401	Implementation of smart hearing aid using TMS320C6713	Functional	Hearing impairment significantly reduces speech perception, especially in noisy environments where traditional analog hearing aids amplify both speech and background noise uniformly. To address these limitations, this project implements a Smart Hearing Aid using the TMS320C6713 DSP Kit, which performs real-time digital filtering to enhance speech clarity. A 63-tap Hamming-window FIR band-pass filter (300 Hz–3.4 kHz), generated using Python, is deployed on the DSP. The TLV320AIC23 codec samples speech at 48 kHz, while the TMS320C6713 executes floating-point convolution with circular buffering to ensure stable, low-latency processing (<10 ms). Testing in street, cafeteria, and office environments demonstrated effective suppression of low-frequency and broadband noise. MATLAB-based waveform and spectrogram analysis confirmed an average SNR improvement of approximately 11 dB, with no clipping, buffer overrun, or perceptible delay during real-time operation. These results validate the efficiency of the FIR-based enhancement method and establish a low-cost DSP platform suitable for modern hearing-aid applications, with potential for future upgrades such as adaptive

List of Projects: 2025-26

						filtering, AI-based noise classification, and multi-band processing.
2	EC	Prof.Shivaprasad	4VP22EC005 4VP22EC051 4VP22EC053 4VP22EC055	A Deep Learning Based Fruit And Vegetable Ripeness Recognition And Classification System	Functional	The project presents an automated system to detect and classify the ripeness of bananas and tomatoes that applies deep learning methods. Video footage was taken of each fruit and vegetable across three separate stages of ripeness: unripe, ripe, and overripe. The video footage was then processed to allow the frame separations and form the dataset used for training and testing purposes. The images were separated to train a Neural Network (NN) and Convolutional Neural Network (CNN) to classify the images into the previous ripeness categories. A program was developed to test the models and used metrics and confusion matrices to assess model performance based on a framework of accuracy, precision, recall, and F1-score. Furthermore, a situation of real-time detection was created using a mobile camera to identify the level of ripeness with fruit and vegetables in real-time. This thorough process demonstrates the feasibility of using deep learning to monitor fruit and vegetable quality in a manner that is doable, verifiable, scalable, and less time-consuming than manual assessment, ultimately supporting applications in agricultural production and the food supply chain.

List of Projects: 2025-26

3	EC	Prof. Nisha G.R	4VP22EC031 4VP22EC039 4VP22EC045	ProtoLink-CAN: An FPGA–Microcontroller Based Custom CAN Communication Framework	Functional	The ProtoLink CAN project is an educational hardware initiative aimed at providing practical understanding of embedded communication systems through the implementation of a simplified CAN-like architecture. The work combines foundational concepts of digital logic with microcontroller-based sensing and actuation to create a clear, hands-on learning environment. Using the Basys-3 FPGA, the project demonstrates how identifier bits, data fields, and error conditions can be manually constructed and visualized on seven-segment displays, helping learners understand frame structure, switching logic, and real-time hardware behaviour. Complementing this, the ESP32 subsystem illustrates essential communication principles by reading a potentiometer through its ADC, transmitting the measured values over a differential physical layer using MCP2551 transceivers, and reproducing the results on an LCD while controlling a DC motor through PWM. This two-part approach bridges theoretical learning with practical execution, allowing students to observe sensing, communication, and actuation as a continuous process. Overall, the ProtoLink CAN project reinforces core concepts in embedded systems, digital logic, hardware interfacing, and real-time communication design,

						offering a clear and effective platform for practical learning.
4	EC	Prof. Rajani Rai B	4VP22EC037 4VP22EC048 4VP22EC052 4VP22EC060	Braille Script Character Recognition & Classification Using Deep Learning	Functional	The Braille Script Character Recognition and Classification System using Deep Learning is designed as an intelligent assistive technology to aid visually impaired individuals by automating the recognition and interpretation of Braille characters. The system captures high-resolution images of Braille scripts using a camera module and processes them through a detailed image preprocessing pipeline comprising grayscale conversion, adaptive thresholding, noise reduction, and contour detection to accurately isolate Braille dot patterns. A custom-designed Convolutional Neural Network (CNN) is trained to classify numerical Braille characters (0–9) and achieves a test accuracy of 94.8%, demonstrating strong robustness, reliability, and generalization performance. Following classification, the recognized character is transmitted wirelessly to a tactile output unit, where an array of servo motors physically reconstructs the corresponding Braille dot configuration, enabling users to perceive the output through touch in real time. The seamless integration of deep learning–based image recognition with embedded hardware ensures fast inference, low latency, and consistent performance under varying lighting and environmental

						conditions. Overall, the proposed system provides a cost-effective, efficient, and user-friendly solution that enhances Braille accessibility, bridges the communication gap between visually impaired and sighted individuals, and offers scalability for future enhancements such as full four-dot Braille implementation, alphabet recognition, and advanced wireless communication features.
5	EC	Prof. Sowmya Anil	4VP22EC016 4VP22EC021 4VP22EC028 4VP22EC047	Phase Locked Loop For Wireless Communication	Functional	PLLs are critical components in modern communication and electronic systems owing to their ability to provide stable frequency synthesis, clock generation, and signal synchronization. In contemporary VLSI designs, PLL designs have to be developed for low power consumption, high operating frequency, enhanced stability, and compact area as well. But most of the existing PLL architectures show difficulties in reducing jitter, providing fast locking, and obtaining a wide tuning range, mainly when these PLL architectures have been realized in deep submicron CMOS technologies.In this project, a Type-II, third-order PLL architecture using the 45 nm CMOS process is proposed. The PLL consists of a Phase Frequency Detector, Charge Pump, passive Loop Filter, and a Current-Starved VCO. Based on the observation that precise phase

						comparison and controlled current injection significantly improve locking behavior, the PFD and CP are optimized to reduce mismatch and dead-zone effects. The loop filter generates a stable control voltage, and the current-starved VCO provides a wide tuning range in the GHz region. The PLL achieves lock by continuously comparing the reference and feedback signals, adjusting the VCO frequency until both signals match in phase and frequency.The fast locking, low power consumption, and high-frequency operation make the proposed system suitable for wireless communication and high-speed digital applications. Simulation results confirm that the PLL locks at 4.8 GHz for a 100 MHz reference input with a VCO gain of 500 MHz/V. The robustness in process, voltage, and temperature variations is also maintained within the design, operating stably under different conditions. Experimental analysis supports the efficiency and performance of the proposed PLL architecture.
6	EC	Prof.Mahabaleshwara Bhat P	4VP22EC049 4VP22EC022 4VP22EC013 4VP22EC040	Low-cost, portable and power efficient ECG Signal Analysis and Heartbeat sound Acquisition System for Cardiac Assessment	Functional	The proposed system presents a low-cost, portable device for the real-time, dual-signal acquisition and analysis of cardiac activity. By integrating electrocardiogram (ECG) and phonocardiogram (PCG) monitoring, the system provides a holistic preliminary assessment tool designed for accessibility

						and intelligent health monitoring. Utilizing a dual-processor architecture for signal processing and user interface, the system's key innovation is the deployment of on-device machine learning for real-time arrhythmia classification, eliminating the need for cloud connectivity. The prototype delivers immediate visual and auditory feedback through a live ECG display and amplified heart sounds, all powered by an efficient power management scheme to enable prolonged use in diverse clinical and remote settings.
7	EC	Prof.Shivaprasad	4VP22EC041 4VP22EC057 4VP22EC405	Active Noise Cancellation Using Adaptive Signal Processing For Industrial Application	Functional	Active Noise Cancellation (ANC) is an effective technique for reducing unwanted low- frequency noise using adaptive signal processing.Project presents a MATLAB-based implementation of an adaptive ANC system using the Filtered-x Least Mean Square (FxLMS) algorithm.The system adaptively generates an anti-noise signal to minimize the residual error in the presence of time-varying noise.Active Noise Cancellation (ANC) is an advanced technique that reduces noise by generating a secondary anti-noise signal. ANC works on the principle of destructive interference, where sound waves of equal amplitude and opposite phase cancel each other. Modern ANC systems use adaptive filtering algorithms to handle time-varying noise

						conditions. Key performance factors include convergence speed, computational cost, and noise reduction performance.The proposed ANC system is adaptive in nature, allowing it to continuously adjust filter coefficients based on the error signal.A software-based MATLAB simulation provides a cost-effective and flexible platform to analyze ANC behavior before real-time hardware implementation.This project implements an adaptive ANC system using the FxLMS algorithm in MATLAB.
8	EC	Prof Akshay S P	4VP22EC015 4VP22EC023 4VP22EC014 4VP22EC038	Bit Data Resolver	Functional	This project presents the design and implementation of the "Bit Data Resolver," an FPGA-based real-time error detection and correction system utilizing a Cyclic Redundancy Check algorithm on a programmable logic platform. The system employs a parallel computation engine that processes data words within a single clock cycle, achieving deterministic latency and high throughput while ensuring robust data integrity in digital communication channels. The implemented design demonstrates full detection and correction accuracy for individual errors and incorporates configurable error injection mechanisms for comprehensive testing. Performance analysis highlights efficient operational frequency, low power consumption, and optimized hardware resource utilization. Furthermore,

						the system successfully detects multiple error classifications, including burst errors, delivering rapid data transfer rates with minimal latency, rendering it suitable for telecommunications, industrial automation, automotive systems, and aerospace applications where data reliability is critical.
9	EC	Prof.Mahabaleshwara Bhat P	4VP22EC007 4VP22EC011 4VP22EC054 4VP22EC058	Enhanced Bank Locker Security System	Functional	This project presents the design and implementation of an enhanced bank locker security system that integrates IoT, biometrics, and AI-based technologies to ensure robust multilayer authentication and intelligent surveillance. The proposed system employs RFID authentication as the primary access level, followed by OTP verification, fingerprint scanning, and facial recognition to guarantee that only authorized individuals can access the locker. Additionally, an AI-powered surveillance module continuously monitors activity around the locker and detects suspicious behaviour using real-time image analysis. All authentication data, logs, and video evidence are securely stored on Supabase cloud storage for remote access and monitoring. The system combines the ESP32, IP-CAM, Raspberry Pi, and various sensors to create a reliable and scalable smart locker solution. Experimental results show that the system provides accurate recognition, rapid response, and enhanced safety compared to conventional single-factor authentication

						systems. This integrated approach represents a significant step toward the modernization of physical asset protection in the banking sector.
10	Ec	Prof. Shreyas H	4VP22EC010 4VP22EC034 4VP22EC042 4VP22EC044	Smartphone Controlled Robotic Arm	Functional	The smartphone-controlled robotic arm is a compact mechatronic system designed to demonstrate remote manipulation using wireless communication. The project integrates a mobile application, Bluetooth connectivity, an ESP32 microcontroller, servo actuators, and a 3D-printed mechanical structure to create an intuitive and flexible control platform. Users can operate the robotic arm by sending joint-angle commands directly from a smartphone interface, enabling precise movement of the base, shoulder, elbow, wrist, and gripper.The system architecture supports real-time control, smooth servo operation, and customizable motion sequences, making it suitable for educational, industrial, and research applications. The project highlights the effective use of low-cost components to achieve reliable robotic motion, offering an accessible approach to human–machine interaction. Future enhancements may include closed-loop feedback, inverse kinematics, advanced trajectory planning, and vision-based automation, enabling the

						robotic arm to perform more complex tasks with higher accuracy and autonomy. Furthermore, the system emphasizes modularity in both hardware and software design. The mechanical components are fabricated using lightweight 3D-printed parts, allowing easy customization, maintenance, and scalability. The control firmware is developed on the ESP32 platform, providing a robust environment for real-time processing, Bluetooth communication, and servo signal generation. The smartphone application acts as a user-friendly interface that enables seamless interaction without requiring specialized equipment, making the system accessible to beginners and efficient for rapid experimentation. Overall, this project demonstrates how modern embedded systems and wireless technologies can be combined to create an interactive robotic platform suitable for automation, education, and prototyping. The smartphone-controlled robotic arm serves as a practical foundation for future advancements such as autonomous pick-and-place operations, machine learning-based control, sensor integration, and multi-axis coordination. By bridging mobile technology with robotics, the system offers a versatile and scalable solution for remote manipulation tasks in various real-world

						applications.
11	EC	Dr. Shrikanth Rao S K	4VP22EC002 4VP22EC003 4VP22EC004 4VP22EC019	Digitization and classification of ECG images	Functional	Electrocardiogram (ECG) analysis is a key technique for diagnosing heart disorders. This project is complete framework for digitizing and classifying ECG images using machine learning methods. The system converts ECG images into digital data. It then preprocesses the data, filters out noise, detects peaks, extracts features, and also uses dimensionality reduction technique namely Principal Component Analysis (PCA). Time-domain and nonlinear features are extracted to measure heart variability. Traditional machine learning classifiers and ensemble machine learning classifiers with tenfold cross-validation are used for performance comparison. The RF classifier achieved the highest accuracy of 65.93% and an F1-score of 0.64. It outperformed the other models in both stability and reliability. The proposed automated ECG interpretation framework shows the potential of combining feature engineering with traditional machine learning techniques for effective detection of heart abnormalities and digital health management.
12	EC	Prof. Akshay S P	4VP22EC035 4VP22EC029 4VP22EC043 4VP23EC403	Design of RISC Processor	Functional	This project presents the comprehensive design and implementation of an 8-bit Reduced Instruction Set Computer (RISC) processor featuring a 5-stage pipeline architecture, aimed at creating a simplified

						yet functional processor suitable for educational use. The architecture is structured into five stages—Instruction Fetch (IF), Instruction Decode (ID), Execute (EX), Memory Access (MEM), and Write Back (WB)—which together enable parallel instruction execution and improved throughput without increasing clock frequency. Core components such as the ALU, control unit, register file, and instruction decoder were designed and integrated in Verilog HDL, following RISC principles of a streamlined and fixed-length instruction set. Simulation results validated the correct execution of instructions and effective functioning of the pipeline along with its hazard mitigation mechanisms. Although the full 8-bit processor was completely verified through simulation, its hardware realization on the Basys-3 FPGA was limited to a 4-bit ALU, which served as a practical proof-of-concept demonstrating correct ALU behavior on real FPGA hardware. Overall, the work successfully demonstrates the complete digital design flow of a pipelined RISC processor—from architectural specification to post-implementation simulation bridging theoretical concepts with practical CAD-based verification, and establishing a strong foundation for future

						full-scale FPGA implementation of the entire 8-bit system.
13	EC	Dr. Shrikanth Rao S K	4VP22EC030 4VP22EC026 4VP22EC046 4VP23EC400	Exam Fees Payment Student Kiosk	Functional	The Exam Fee Payment Kiosk System presented in this project is a modern, fully digital solution designed to simplify and automate the process of examination fee payment in educational institutions. The project utilizes a web-based architecture built with React (Frontend) and Node.js/Express (Backend), making it more flexible, scalable, and visually dynamic. Students begin the payment process by entering their USN and semester on a large touchscreen interface, enhanced with a custom-built virtual touch keyboard optimized for kiosk displays. The system automatically fetches verified student details—including name, branch, and fee amount—from a centralized backend database, ensuring accuracy and eliminating manual entry errors. Once student information is confirmed, the system integrates with Zerotize, a secure and reliable payment gateway, to generate a real-time UPI/QR-based payment session. After completing the payment, students enter their UTR number, which is cross-checked live with Zerotize's verification API. Upon successful verification, the kiosk instantly generates a digital and printable receipt containing all transaction details such as date, time, and payment ID. Additionally, features

						such as auto-slideshow screens, smooth animations, touch optimized UI, and automatic printing enhance usability and accessibility. By automating fee collection, reducing manual workload, eliminating queues, and enabling secure cashless payments, this Exam Fee Payment Kiosk System represents a significant advancement toward a smarter and more efficient educational ecosystem. Its modular, scalable architecture ensures long-term adaptability, supporting future expansions like attendance tracking, hall ticket printing, and online student services.
14	EC	Prof.Prbha G S	4VP22EC017 4VP22EC050 4VP23EC402 4VP23EC406	Smart Shopping Trolley With Automated Billing and QR Based Checkout System	Functional	In today's world of rapidly growing population and diverse consumer demands, retail environments such as supermarkets face significant challenges, including long checkout queues, inefficient product coordination, and time-consuming shopping processes. Customers often spend considerable time navigating stores and managing their purchases manually. With continuous advancements in automation and IoT, there is a strong need for intelligent systems that simplify shopping and improve customer experience. To address these issues, smart technologies especially autonomous mobility features such as line-following mechanisms play a crucial role in enhancing convenience and reducing manual effort for

						shoppers. The project, titled "Smart Shopping Trolley with Automated billing and QR Based Checkout System" This system integrates intelligent mobility, automated product tracking, and real-time billing to enhance customer convenience and efficiency. The trolley incorporates a line-following mechanism along with ultrasonic obstacle detection, enabling it to autonomously follow the customer and navigate safely within the store environment. A QR code scanning unit allows customers to instantly add or remove items from their virtual cart by scanning the QR codes on products. To ensure compatibility with all items, the system also features virtual QR code generation for products that lack printed codes. An embedded controller, such as Raspberry Pi, processes all scanned product data and updates the bill in real time through a onboard display. By providing automated checkout and seamless digital payment, the smart trolley significantly reduces human effort, eliminates long queues, and improves overall shopping efficiency.
15	EC	Prof.Nithin	4VP22EC027 4VP22EC001 4VP22EC012 4VP22EC032	Smart Intruder Detection and Security System	Functional	Intrusion detection is a critical requirement for ensuring the safety and security of homes and restricted premises. This project presents a complete framework for designing and implementing a Smart Intruder Detection System using Internet of Things (IoT)

						technologies. The proposed system monitors unauthorized access and lock-tampering activities using a vibration sensor interfaced with a Raspberry Pi. Sensor data are continuously acquired, processed, and analyzed to detect abnormal vibration patterns indicative of intrusion attempts. Upon detection, the system immediately generates real time alerts through a Wi-Fi-based Telegram bot to a registered smartphone. To enhance reliability, a GSM module with a dedicated backup battery is integrated to ensure uninterrupted alert transmission during network or power failures. The system emphasizes low cost, scalability, and ease of deployment while maintaining high responsiveness and accuracy in intrusion detection. Experimental results demonstrate that the proposed framework provides timely notifications, robust fault tolerance, and effective security monitoring, making it suitable for smart home and small-scale security applications.
16	EC	Prof.Prabha G S	4VP22EC025 4VP22EC024 4VP22EC056 4VP22EC059	Power efficient VLSI design of an optimized MAC unit	Functional	The Multiply–Accumulate (MAC) unit is a critical component in modern digital systems. It performs repetitive operations of the form A×B+C. These operations are widely used in image processing, communication systems, artificial intelligence, and signal processing. Conventional MAC designs rely on array multipliers and ripple-carry or carry-

						lookahead adders. These traditional architectures often suffer from higher delay. They also consume more power due to excessive switching activity. Such limitations create challenges for power-constrained devices. To overcome these issues, a power-efficient MAC unit is proposed. This design uses a Vedic Multiplier based on the Urdhva–Tiryagbhyam algorithm. The Vedic method generates partial products in parallel. This significantly reduces multiplication delay. A Carry Select Adder (CSelA) is included to minimize carry propagation time. Clock-gating techniques are implemented to reduce unnecessary dynamic power consumption. The design is implemented using Verilog HDL on the Basys 3 FPGA. Experimental results from Xilinx Vivado show improved power and timing performance. Hardware testing confirms that the proposed MAC unit is accurate, stable, and efficient for high-speed, low-power applications.
17	EC	Prof Nirupama K	4VP23EC404 4VP22EC033 4VP22EC020 4VP22EC006	Control and Camera based state estimation using Machine Learning and Machine Vision	Functional	Control and Camera based state estimation using Machine Learning and Machine Vision project presents the design and implementation of a self-balancing robot that utilizes machine vision and machine learning techniques for real-time state estimation and control. This project explains how a self-balancing robot is designed using a ESP32 as the main controller. The robot uses an

						MPU6050 sensor to measure tilt, an ultrasonic sensor to detect obstacles, and a Pi Camera for visual input. The ESP32 collects this data through I2C and camera processing to understand the robot's angle and surroundings. Based on this information, the ESP32 controls the motors through an L298N motor driver to keep the robot balanced. Machine learning models are trained using sensor readings and camera images to improve the robot's accuracy and ability to adapt to different conditions. Overall, this system combines machine vision, sensor data, and intelligent control to create a low cost and effective self-balancing robot. The project can be further expanded for advanced robotics where stability and environment understanding are important.